Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.041”**

**ANODE**

**.023 x .023”**

**.041”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .023 X .023”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 10/21/21**

**MFG: SILICONIX THICKNESS .010” P/N: 1N4005**

**DG 10.1.2**

#### Rev B, 7/1